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COBALT SILICIDE FABRICATION METHODS THAT USE PROTECTIVE TITANIUM LAYERS

Vincent Fortin

Kuei-Chang Tsai

BACKGROUND OF THE INVENTION

[0001] The present invention relates to formation of cobalt silicide on a silicon surface.

[0002] Cobalt silicide has been used to reduce the resistance of transistor gates and source/drain regions in silicon integrated circuits. Cobalt silicide can be formed in a self-aligned manner by a "salicide" (self-aligned silicide) process illustrated in Figs. 1 and 2. These figures show a polysilicon gate 100 and source/drain regions 101 of a MOS transistor fabricated in a wafer 102. The source/drain regions 101 are doped regions of a monocrystalline silicon substrate 104. Gate dielectric 108 separates the gate 100 from the substrate. Dielectric spacers 110 cover the sidewalls of gate 100.

[0003] A cobalt layer 120 is sputtered over the structure. A titanium layer 130 is sputtered on cobalt 120 to protect the cobalt layer from oxygen and other impurities during subsequent processing. Then the wafer is heated (in a rapid thermal processing step, or RTP) to react cobalt 120 with the silicon at the top of gate 100 and on source/drain regions 101. A cobalt silicide layer 210 (Fig. 2) forms as a result. This layer may include cobalt monosilicide CoSi and cobalt disilicide $CoSi_2$. Titanium 130 and the unreacted cobalt are removed with a wet etch. The wafer is heated again to increase the proportion of cobalt disilicide $CoSi_2$ in layer 210 and thus reduce the layer 210 resistivity. See H. Liu et al., "Gaseous Impurities in Co Silicidation", Journal of The Electrochemical Society, 148 (6) G344-G354 (2001), incorporated herein by reference.

[0004] In addition to protecting the cobalt layer 120 from impurities, some of titanium 130 may diffuse to the cobalt/silicon interface and dissolve the native silicon oxide, thus allowing the cobalt silicide to form (the cobalt itself does not dissolve the native oxide).

[0005] The cobalt salicide process has been suggested for silicidation of silicon surfaces at the bottom of openings formed in dielectric layers deposited over silicon. When cobalt 120 is deposited in the openings, a good step coverage is needed in order to

have a sufficient cobalt thickness at the bottom of the openings and thus achieve low cobalt silicide resistivity. As the integrated circuit technology is scaled down to smaller line widths, the aspect ratios of the openings tend to increase, and achieving a good step coverage of the cobalt film becomes increasingly difficult. Applied Materials, Inc. has announced that its Endura® ALPS™ (Advanced Low Pressure Source) cobalt deposition chamber can provide greater than 10% bottom coverage in 6:1 aspect ratio contact openings. Further improvements in the cobalt silicide fabrication are desirable.

SUMMARY

[0006] The invention is defined by the appended claims which are incorporated into this section in their entirety. The rest of this section summarizes some features of the invention.

[0007] The inventors have observed that the cobalt salicide process needs not only a good step coverage of cobalt 120 but also a good step coverage of titanium 130. Fig. 3 illustrates an opening 310 formed in dielectric 320 over substrate 104. Cobalt 120 and titanium 130 have been deposited over the dielectric as in Fig. 1. Titanium 130 has to be sufficiently thick to protect the cobalt 120 from the gaseous impurities. If the titanium step coverage is poor, i.e. the titanium is thinned in bottom corners 310C, then the titanium thickness T as measured over the non-stepped surfaces has to be increased. If the step coverage is good, the titanium thickness can be less, resulting in a better process control and lower "cost of ownership" (overall manufacturing cost).

[0008] In some embodiments of the invention, the titanium is deposited by ionized physical vapor deposition process ("ionized PVD"). An ionized PVD chamber includes an induction coil positioned between the titanium target and the wafer. The coil is energized with an AC current to densify the plasma in the chamber. As the sputtered titanium atoms move towards the wafer, some of the titanium atoms become ionized due to the coil energy. The pedestal holding the wafer is also biased with an AC current to attract the titanium ions and cause them to approach the wafer at an angle closer to 90°. See "Handbook of Semiconductor Manufacturing Technology" (edited by Yoshio Nishi et al., 2000), pages 406-407, incorporated herein by reference. Better step coverage is achieved at the bottom of the openings because the ions approaching the wafer at the angles near 90° are less likely to create overhangs near the top of the openings.

[0009] In some embodiments of the invention, however, the wafer holding pedestal bias is turned off to reduce cobalt resputtering and thus achieve a lower cobalt silicide resistance.

[0010] Also, in some embodiments, the titanium deposition is performed in a medium or long throw chamber (the throw is the distance between the titanium target and the wafer). In some embodiments, the throw is at least 140 mm. Better step coverage is achieved because the titanium atoms and ions reaching the wafer are more likely to be closer to normal incidence. See "Handbook of Semiconductor Manufacturing Technology" (edited by Yoshio Nishi et al., 2000), page 402, incorporated herein by reference.

[0011] Other features of the invention are described below. The invention is defined by the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figs. 1-3 are cross section illustrations of prior art semiconductor structures.

[0013] Fig. 4 shows a cross section of an ionized PVD chamber suitable for forming cobalt silicide according to some embodiments of the present invention.

[0014] Fig. 5 is a circuit diagram of a memory array fabricated according to one embodiment of the present invention.

[0015] Fig. 6 is a top view of the array of Fig. 5.

[0016] Figs. 7A, 7B show vertical cross sections of the array of Fig. 5.

DESCRIPTION OF SOME EMBODIMENTS

[0017] The examples in this section are provided for illustration and not to limit the invention. The invention is not limited to particular deposition parameters, processes, equipment, thickness values or other dimensions, except as defined by the claims.

[0018] In one example, cobalt silicide is formed using a cluster tool of type Endura 5500 available from Applied Materials, Inc. of Santa Clara, California. Optionally, prior to loading the wafers in the Endura tool, a 100:1 HF wet clean can be performed on the wafers to remove the native silicon oxide. In the Endura system, the wafers are submitted to a degas step followed by a sputter-etch step in RF argon plasma to remove the native oxide. The HF cleaning step and the sputter-etch step can be omitted (the

native oxide tends to be dissolved by the titanium atoms diffusing through the cobalt layer) or can be replaced with other cleaning steps.

[0019] Then cobalt is deposited in the Endura cluster tool in a chamber of type ALPS™ (Advanced Low Pressure Source) available from Applied Materials, Inc.. An exemplary cobalt thickness is 20 nm or 40 nm, and other thickness values can also be used. The deposition parameters and some properties of the resulting cobalt film are given in Table 1. The cobalt film properties were actually obtained for the 20 nm cobalt thickness.

[0020] TABLE 1

Target to Wafer Spacing	about 190 mm
Target Power	about 2 Kw
Chamber Pressure	below 1.0 mTorr
Wafer Chuck Temperature	room temperature

[0021] Then titanium layer 130 is deposited by ionized PVD. In some embodiments, the titanium is deposited *in-situ*, without breaking the vacuum after the cobalt deposition and without unloading the wafer from the Endura cluster tool, and the deposition is performed in a medium throw magnetron IMP (ion metal plasma) chamber 410 (Fig. 4) of type Vectra available as part of the Endura tool. Titanium target 420 is shown mounted at the top of chamber 410. Target 420 is connected to a negative DC bias source 430. Wafer 102 is placed on a metallic pedestal 440. Bias source 450 biases the pedestal with an AC current of a frequency 13.56MHz. Argon is flown into the chamber. Bias source 430 helps ionize the argon. Coil 460 generates an RF electromagnetic field to densify the argon plasma, making the plasma high density. The argon ions dislodge titanium atoms from target 420. Some of the titanium atoms become ionized by the high density plasma. The titanium atoms and ions settle on wafer 102. See "Handbook of Semiconductor Manufacturing Technology" (edited by Yoshio Nishi et al., 2000), pages 395-413, incorporated herein by reference.

[0022] The throw distance (the distance between target 420 and wafer 102) is 140 mm.

[0023] In some embodiments, the titanium is deposited with the AC pedestal bias turned off (0 W). Other deposition parameters can be as follows:

[0024] TABLE 2

DC power on target (source 430)	2 kW
RF power (coil 460)	2.5 kW
AC pedestal bias (source 450)	0 W
DC voltage at the pedestal	0 V
Pressure in chamber 410	18 mTorr
Argon flow	60 sccm
Temperature in chamber 410	200°C

[0025] An exemplary thickness of titanium layer 130 is 7.5 nm or less. Thickness above 7.5 nm, for example, 15 nm or 25 nm, can also be used.

[0026] Then the wafer is unloaded from the Endura tool and annealed in a Rapid Thermal Annealing (RTA) system to form cobalt silicide. In one example, the anneal involves holding the wafer at 550°C for 30 seconds in a nitrogen atmosphere. The nitrogen flow is 5 slm (standard liters per minute). Suitable equipment is HEATPULSE 8800 available from AG Associates, Inc., of San Jose, California. Other equipment and anneal parameters can also be used.

[0027] The anneal is followed by selective wet strips of the titanium 130 and the unreacted cobalt. In one example, the titanium is stripped by a 5 minute etch in a solution consisting of 1 part of NH_4OH, 1 part of H_2O_2, and 2 parts of water. The cobalt is stripped by a 5 minute etch in a solution of 10 parts of H_2SO_4 and 1 part of H_2O_2. Finally, the wafers are subjected to another RTA step (e.g. 30 seconds at 800°C with a nitrogen flow of 5 slm in a HEATPULSE 8800 chamber) to form the low-resistivity $CoSi_2$ phase. The above wet etch and anneal parameters are exemplary and not limiting.

[0028] In one example, cobalt silicide is formed on the source lines of a flash memory array illustrated in Figs. 5-8. Some features of this memory are described in U.S. patent application no. 09/640,139 filed August 15, 2000 by Hsing Tuan et al., entitled "Nonvolatile Memory Structures and Fabrication Methods", incorporated herein by reference. Fig. 5 is a circuit diagram showing two columns of the array. Fig. 6 is a top view. Fig. 7A illustrates a cross section of the array along the line A-A in Fig. 6. Fig. 7B illustrates a cross section along the line B-B.

[0029] The array is fabricated over a P- type doped region of a monocrystalline silicon substrate 104 (Figs. 7A, 7B). Silicon dioxide 508 ("tunnel oxide") is formed on substrate 104. Polysilicon floating gates 524 are formed on oxide 508.

[0030] Dielectric 526 (Figs. 7A, 7B) separates the floating gates from control gates 528. In each memory row, the control gates are provided by a line of doped polysilicon ("control gate line"). The control gate lines are referenced as 528, like the individual control gates. Control gate lines 528 are vertical lines in Figs. 5 and 6.

[0031] Silicon nitride 530 overlies control gate lines 528. Oxide 508, polysilicon 524, dielectric 526, control gate lines 528, and silicon nitride 530 form a stack 532 in each row of the array. Each stack 532 traverses the entire array, except that the floating gates 524 of different memory cells are separated from each other.

[0032] Dielectric 534 (Figs. 7A, 7B) on the sidewalls of stacks 532 insulates the control and floating gates from polysilicon wordlines 536. In some embodiments, dielectric 534 includes silicon dioxide (not separately shown) formed on the sidewalls of polysilicon 524, 528, and also includes an outer layer consisting of silicon nitride spacers which overly the silicon dioxide. A thin silicon dioxide layer 535 (Fig. 7A) is formed on the substrate under the dielectric 534.

[0033] Each wordline 536 is a spacer on a sidewall of a stack 532. Each wordline runs vertically in the view of Figs. 5 and 6 and provides select gates for one row of the array.

[0034] Each memory cell 538 has source/drain regions 542, 544 in substrate 104 (Figs. 5, 7A). Region 542 ("bitline region") is adjacent to select gate 536 and is connected to a bitline 546 (Figs. 5, 6). The bitlines go over the control gate lines 528, silicon nitride 530, and wordlines 536. Each column of the memory cells is connected to one bitline. Each bitline region 542 is shared by two memory cells in adjacent rows. Bitline regions 542 are connected to the bitlines by contacts 548. Each contact is a conductive structure that passes through one or more dielectric layers (not shown).

[0035] A thin silicon dioxide layer 550 is shown to overly the bitline regions 542. This layer is removed during the formation of the contact openings for contacts 548.

[0036] Regions 544 ("source line regions") are formed on the opposite side of each stack 532 from regions 542. Two adjacent rows have their regions 544 merged into a contiguous diffused "source line" that transverses the array between two respective stacks 532.

[0037] Cobalt silicide 210 is formed on source lines 544 by any of the processes described above. Cobalt silicide 210 can also be formed on wordlines 536.

Alternatively, the wordlines can be covered by a dielectric (not shown) during the cobalt deposition, so cobalt silicide will not form on the wordlines.

[0038] Isolation trenches 560 (Figs. 6, 7A, 7B) in substrate 104 are filed with dielectric 564 ("field oxide"), which is silicon dioxide in some embodiments. Dielectric 564 provides isolation between the active areas of the memory array. The trench boundaries are shown at 560B in Fig. 6. The trenches extend in the bitline direction between adjacent source lines 544. Each trench 560 passes under two rows of the array and projects from under the respective control gate lines 528 into the source lines.

[0039] In Fig. 5, each cell 538 is schematically represented as an NMOS transistor and a floating gate transistor connected in series. Each row of memory cells has two cells 538 between each two adjacent bitlines 546.

[0040] Exemplary voltages for the programming, erase and reading operations of the memory are described in the aforementioned U.S. patent application no. 09/640,139.

[0041] In some embodiments, the height of each stack 532 is about 0.48 μm in the cross section of Fig. 7A. Each cobalt silicide line 210 extends between two dielectric features 534. The width of each line 210 in the cross section of Fig. 7A is about 0.30 μm to 0.38 μm. The aspect ratio of the opening into which the cobalt and titanium layers are deposited during the fabrication of cobalt silicide 210 (the opening between adjacent stacks 532) is thus about 1.3 to 1.6. The width of each dielectric feature 534 at the bottom is about 0.02 μm to 0.06 μm.

[0042] In the cross section of Fig. 7B, the height of each stack 532 is about 0.3 μm. The width of the cobalt silicide line 210 is about 0.13 μm to 0.21 μm. The aspect ratio is thus about 1.6 to 2.5. The width of each dielectric feature 534 at the bottom is about 0.02 μm to 0.06 μm.

[0043] These dimensions are exemplary and not limiting. Cobalt silicide can be formed in openings having any aspect ratios. Aspect ratios of 2.5, 2.6 and higher are being considered and are not limiting. The invention is not limited by the particular materials, circuits, dimensions, and process parameters described above. For example, the invention is not limited to memories or to the use of silicon dioxide or silicon nitride insulators. The invention is defined by the appended claims.